AMENDMENTS TO THE CLAIMS

1-19. (Cancelled)

20. (Currently Amended) A method of producing a crystalline substrate based device comprising:

providing a wafer ~~comprising a semiconductor microstructure~~ including a semiconductor substrate and comprising a plurality of semiconductor microstructures including at least one optoelectronic device;

providing at least one wafer-level transparent packaging layer;

forming onto said at least one wafer-level transparent packaging layer, a wafer-level ~~providing a~~ spacer ~~at a wafer level~~, said packaging layer and said spacer defining a plurality of cavities ~~at least one cavity~~ extending entirely ~~there~~through said spacer;

~~adhesively~~ sealing ~~to~~ said wafer-level ~~at least one transparent chip scale packaging layer and said~~ spacer to ~~onto~~ said semiconductor substrate ~~over said microstructure and at least partially spaced therefrom~~, thereby fully defining a ~~to define at least one~~ gap ~~at said at least one cavity~~ between ones of said plurality of microstructures and corresponding ~~said at least one~~ chip scale portions of said at least one transparent packaging layer, without requiring removal of material from said at least one transparent packaging layer overlying said at least one optoelectronic device; and

~~forming a multiplicity of electrical contacts along surfaces of said at least one packaging layer which define edges of individual chip scale packaged devices; and~~

subsequently dicing said semiconductor substrate, having said wafer-

level spacer and said at least one wafer-level transparent packaging layer sealed thereunto, to form ~~into said~~ individual chip scale packaged devices~~,~~

~~wherein said spacer is formed as a piece separate from said substrate~~.

21. (Cancelled)

22. (Currently Amended) A method of producing a crystalline substrate based device according to claim 20 and wherein said ~~adhesively~~ sealing comprises using Epoxy to seal ~~said at least one transparent chip scale packaging layer and~~ said wafer-level spacer onto said semiconductor substrate.

23. (Currently Amended) A method of producing a crystalline substrate based device according to claim 20 and wherein said semiconductor ~~crystalline~~ substrate comprises silicon.

24. (Currently Amended) A method of producing a crystalline substrate based device according to claim 20 and wherein said semiconductor ~~crystalline~~ substrate comprises lithium niobate.

25-26. (Cancelled)

27. (Currently Amended) A method of producing a crystalline substrate based device according to claim 20 and wherein said plurality of semiconductor microstructures comprises at least one micromechanical structure.

28. (Currently Amended) A method of producing a crystalline substrate based device according to claim 20 and wherein said plurality of semiconductor microstructures comprises at least one microelectronic structure.

29-32. (Cancelled)

33. (Currently Amended) A method of producing a crystalline substrate based device according to claim 20 and wherein said semiconductor ~~crystalline~~ substrate comprises lithium tantalate.

34. (Currently Amended) A method of producing a crystalline substrate based device according to claim 20 and wherein said plurality of semiconductor microstructures comprises at least one surface acoustic wave device.

35. (Cancelled)

36. (Currently Amended) A method of producing a crystalline substrate based device according to claim 20 and wherein said semiconductor ~~crystalline~~ substrate comprises quartz.

37-38. (Cancelled)

39. (Currently Amended) A method of ~~for~~ producing a crystalline substrate based

device according to claim 20 ~~comprising:~~

~~forming a microstructure on a crystalline substrate; and~~

~~sealing at least one transparent chip scale packaging layer over said microstructure by means of an adhesive so as to define therewith at least one gap between said crystalline substrate and said at least one chip scale packaging layer, said substrate, said microstructure and said chip scale packaging layer forming a chip scale package,~~

wherein said plurality of semiconductor microstructures receives light via said at least one transparent ~~chip scale~~ packaging layer.

40. (Currently Amended) A method of ~~for~~ producing a crystalline substrate based device according to claim 39 and wherein said sealing comprises ~~at least one chip scale packaging layer is sealed onto said crystalline substrate~~ using an adhesive to seal said wafer-level spacer onto said semiconductor substrate.

41. (Currently Amended) A method of ~~for~~ producing a crystalline substrate based device according to claim 40 and wherein said adhesive comprises epoxy.

42. (Currently Amended) A method for producing a crystalline substrate based device according to claim 39 and wherein said semiconductor ~~crystalline~~ substrate comprises silicon.

43. (Cancelled)

44. (Currently Amended) A method of ~~for~~ producing a crystalline substrate based device according to claim 39 and wherein said plurality of semiconductor microstructures comprises at least one micromechanical structure.

45. (Currently Amended) A method of ~~for~~ producing a crystalline substrate based device according to claim 39 and wherein said plurality of semiconductor microstructures comprises at least one microelectronic structure.

46. (Cancelled)

47. (Currently Amended) A method for producing a crystalline substrate based device according to claim 39 and wherein said semiconductor ~~crystalline~~ substrate comprises lithium tantalate.

48. (Currently Amended) A method for producing a crystalline substrate based device according to claim 39 and wherein said plurality of semiconductor microstructures comprises at least one surface acoustic wave device.

49. (Currently Amended) A method for producing a crystalline substrate based device according to claim 39 and wherein said semiconductor ~~crystalline~~ substrate comprises quartz.

50. (Currently Amended) A method for producing a crystalline substrate based device according to claim 39 and wherein said semiconductor ~~crystalline~~ substrate comprises

lithium niobate.

51-64. (Cancelled)

65. (Currently Amended) A method of ~~for~~ producing a crystalline substrate based device according to claim 20 wherein ~~comprising:~~

~~forming a microstructure on a crystalline substrate; and~~

~~sealing at least one chip scale packaging layer over said microstructure and defining therewith at least one gap between said crystalline substrate and said at least one chip scale packaging layer, the crystalline substrate, microstructure and packaging layer forming a chip scale package,~~

the individual chip scale packaged devices have ~~having~~ a multiplicity of electrical contacts plated along edge surfaces thereof.

66. (Cancelled)

67. (Currently Amended) A method according to claim 65 wherein said sealing comprises using ~~chip scale packaging layer is sealed over said microstructure by means of~~ an adhesive to seal said wafer-level spacer onto said semiconductor substrate.